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Research Paper

Enhancing the Optoelectronic and Photovoltaic Performance of Thermally Evaporated TeSn/c-Si Heterojunctions via Thermal Annealing Management

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Abstract

This study used high-vacuum (10^{-5} Torr) thermal evaporation to fabricate a hybrid tellurium-tin/crystalline silicon (TeSn/c-Si) junction. The junction was deposited at room temperature, 323 K, and 348 K to evaluate its structural and electrical properties. Thin TeSn layers (500 nm thick) and the resulting diodes underwent thermal annealing. DC conductivity testing revealed a double-transfer mechanism governed by the Arrhenius equation. A significant increase in the activation energies E_{a1} and E_{a2} was observed following thermal annealing at 348 K, reaching 0.44 eV and 0.65 eV, respectively. This indicates an improvement in the layer's crystallinity due to annealing and a decrease in the density of local states. Capacitance-voltage (C-V) measurements confirm the formation of a sharp heterojunction interface, exhibiting a significant improvement in the internal potential (V_{bi}) from 1.24 eV (at room temperature) to 1.7 eV (at 348 K) due to the passivation of the interface states. Furthermore, the current-voltage (I-V) characteristics in darkness show thermal emission behavior under forward bias and a gradual breakdown under reverse bias. Under illumination, the heterojunction exhibited a significant improvement in photovoltaic performance, with a peak short-circuit current density (Jsc) of 3.1×10^{-1} mA/ cm^2 after annealing at 348 K. These results highlight the crucial role of post-deposition thermal tuning in reducing recombination centers and enhancing the overall efficiency of chalcogenide-based solar harvesting devices.

Keywords

TeSn Thin Films, Heterojunction, Thermal Annealing, Activation Energy, Built-in Potential, Photovoltaic Performance

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1. INTRODUCTION

Over the last few decades, scientists and industry professionals have shown complementary levels of interest in chalcogenide materials. The interest was likely due to the impressive attributes of chalcogenides, such as adjustable bandgaps and high carrier mobilities and structural flexibility (Scottmiller et al., 1970; Suh et al., 1985; Gravesteijin, 1988; Carcia et al., 1988; Rubin and Chen, 1989). Among these, Tellurium-Tin (TeSn) thin films show potential as a class of binary chalcogenide semiconductors used in IR sensors, optical memory devices, and photovoltaics. The fabrication of hybrid heterojunctions by integrating chalcogenide thin films with single-crystal silicon (c-Si) substrates offers a viable route to high-efficiency, cost-effective solar cells, leveraging the well-established infrastructure of silicon technology (Husain et al., 1998; Pintili et al., 2002).

The chalcogenide glasses are one of the most widely known families of amorphousmaterials and havebeen studied extensively over the past few decades because of their interesting fundamental properties andwide commercial applications. The simple preparation technique of binary and ternary chalcoge nidecompounds as well as their broad range of band gaps, carrier mobilities, transparency in the IR region, and their ability to form various solid-state solutions and to accommodate different dopants have led to their emergence as technologically significant device materials (Zogg, 2006; Ibrahim, 2009; Soundararajan and Mangalaraj, 2021). While previous studies have highlighted the general transport mechanisms in selenium and tellurium-based junctions, a systematic investigation into the correlation between annealing temperatures and the junction parameters specifically the built-in potential (V_{bi}), electrical activation energy (E_a), and illuminated current-voltage (I-V) traits of thermally evaporated TeSn/c-Si heterojunctions remains essential for device optimization (Sze and Ng, 2006; Wang et al., 2023).

In recent years, the optical memory effects in amorphous semiconducting films have been investigated and utilized for various device applications, we investigate the fabrication of a TeSn/c-Si heterojunction via thermal evaporation leveraging

the well-established infrastructure of silicon technology and advanced nanomaterial architectures (Ahmed et al., 2026; Ismail et al., 2025).

We report a detailed analysis of the direct current (D.C.) conductivity and film activation energies as a function of post-deposition annealing temperature (from Room Temperature to 348 K). Furthermore, the junction properties are scrutinized using Capacitance-Voltage (C-V) measurements and Current-Voltage (I-V) characteristics under both dark and illuminated conditions. have recently reported the use of these materials for reversible optical recording using the amorphous to crystalline phase change. Recently attempts have been made by our group to demonstrate the formation of a solar cell using chalcogen elements.

2. EXPERIMENTAL SECTION

2.1 Materials

The study utilized n-type single crystal silicon wafers with a resistivity of 3 Ω · cm and (111) orientation. Chemical solutions: A chemical mixture consisting of hydrofluoric acid, nitric acid, and acetic acid in a volumetric ratio (2HF:3HNO_3:3CH_3COOH mixture (3:5:3). In addition to distilled water, acetone, isopropyl alcohol, and dry oxygen gas.

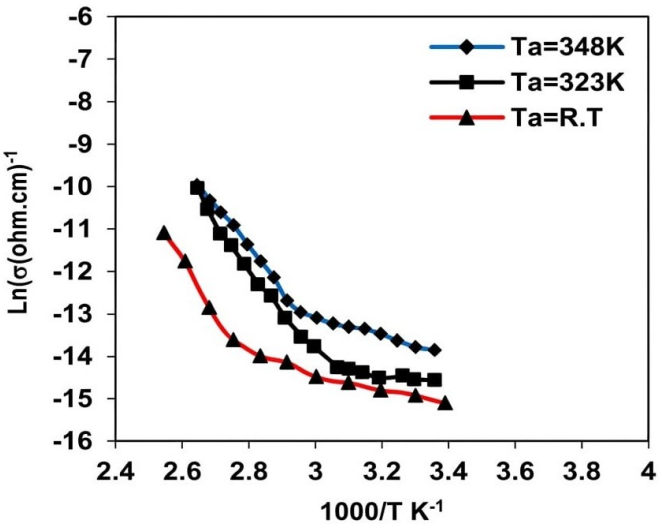

Figure 1. Lnσ as a Function of 1000/T for TeSn/c-si Films

2.2 Method

The wafers were scribed into approximately 1 cm × 0.6 cm pieces, with one surface polished using a. These samples were cleaned ultrasonically by alternating immersion in distilled water, acetone, and isopropyl alcohol. Following cleaning, the samples were oxidized in dry oxygen. Tin-indium (TeSn) films were deposited via thermal evaporation in a vacuum of approximately 10-5 torr at a rate of ~0.8 nm/min onto the polished silicon substrates at room temperature (~300 K). Film thickness was measured using a microbalance method, with a maximum error of about 10% for the thinnest films (500 nm). Ohmic aluminum contacts were thermally deposited on both the silicon and TeSn film sides for electrical measurements. Last steps, the fabricated hybrid junctions were subjected to post-deposition annealing at room temperature, 323 K, and 348 K to optimize junction properties.

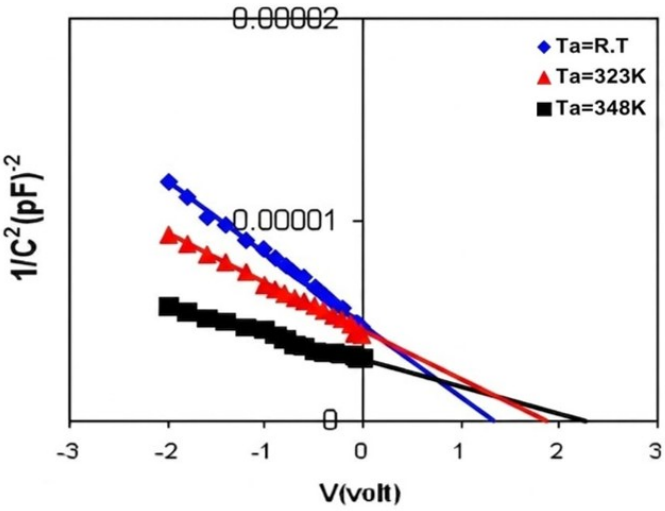

Figure 2. The Variation Capacitance with Voltage for TeSn/Si Hetrojunction at Different Annealing

3. RESULTS AND DISCUSSION

3.1 D.C. Conductivity and Activation Energies of TeSn Layers

The temperature dependence of direct current (D.C.) conductivity ($\sigma_{d.c.}$) for the as-deposited and annealed TeSn thin films was investigated within specific temperature ranges. As illustrated in Figure 1, the plot of lnσ versus 1000/T exhibits two distinct linear regions (a high-temperature region and a low-temperature region). This behavior indicates that the electrical conduction occurs through two different transport mechanisms governed by the well-known Arrhenius relation (Kareem et al., 2020; Sharma and Katyal, 2023).

$$\sigma = \sigma_1 \exp\left(-\frac{E_{a1}}{k_B T}\right) + \sigma_2 \exp\left(-\frac{E_{a2}}{k_B T}\right) \quad (1)$$

where E_{a1} and E_{a2} represent the electrical activation energies for the high and low-temperature regimes, respectively, and k_B is the Boltzmann constant (Wang, 2006; Jassim et al., 2024).

The calculated values of these activation energies at different annealing temperatures (T_a) are summarized in Table 1. For the as-deposited film (at Room Temperature), the activation energies are E_{a1} = 0.2 eV and E_{a2} = 0.33 eV. Upon thermal annealing, a noticeable increase in both activation energies is observed, reaching E_{a1} = 0.44 eV and E_{a2} = 0.65 eV at Ta = 348 K.

This systematic increase in activation energy with annealing temperature can be attributed to the improvement in the film's

Table 1. DC Activation Energy

T_aK	E_{a1} (eV)	Rang Temp. (K)	E_{a2} (eV)	Rang Temp. (K)
R.T	0.2	303-363	0.33	373-483
323	0.32	303-403	0.465	413-483
348	0.44	303-353	0.654	363-483

crystallinity and the minimization of structural defects (Hansen et al., 2010). During thermal annealing, the atomic rearrangement reduces the density of localized states near the valence and conduction band edges. According to recent literature, thermal optimization shifts the Fermi level and broadens the effective optical band gap by removing unsaturated bonds, which consequently demands a higher thermal activation energy for charge carriers to transition between the bands (Baturay et al., 2022).

Table 2. Values of Vbi for TeSn/Si Heterojunction with Different Annealing Temperature

Annealing Temp. (K)	V_{bi} (eV)
R.T	1.24
323	1.4
348	1.7

3.2 Capacitance-Voltage (C-V) Characteristics

To understand the junction configuration and interface quality, the capacitance of the TeSn/n-Si heterojunction was measured as a function of reverse bias voltage. As shown in Figure 2, the linear dependence of $1/C^2$ against the bias voltage (V) confirms that the fabricated device forms an abrupt heterojunction interface , which aligns well with Anderson's theoretical model (Mohammed et al., 2025).

By extrapolating the linear plots of $1/C^2$ to the voltage axis intercept ($1/C^2 = 0$), the built-in potential (V_{bi}) was determined. The extracted Vbi values are detailed in Table 2. It is found that V_{bi} increases significantly with the annealing temperature, rising from 1.24 eV at room temperature to 1.4 eV at 323 K, and further to 1.7 eV at 348 K. This substantial enhancement in V_{bi} is directly linked to the reorganization of the heterojunction interface. As reported by post-deposition thermal treatment passivates the interface traps and reduces the density of surface states (N_{ss}) at the TeSn/c-Si boundaries. The reduction of these interface traps prevents Fermi-level pinning, allowing for a wider depletion region width and a higher barrier height, which is manifests as an increased built-in potential.

3.3 Current-Voltage (I-V) Characteristics in the Dark

The steady-state electrical transport mechanisms of the TeSn/n-Si heterojunction were evaluated through dark current-voltage characterizations. Figure 3 illustrates the dark I-V plots under both forward and reverse bias states for different annealing stages (Kiwi et al., 1994; Ishihara et al., 1998; Anandan et al., 2005; Kumar and Chowdhury, 2017).

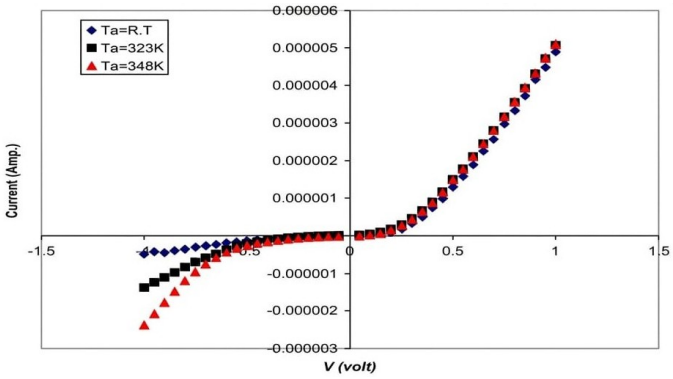

Figure 3. I-V Characteristics in the Dark for TeSn/n-Si Heterojunction at Different Annealing Temperature

In the forward bias direction, the current increases exponentially with the applied voltage. This behavior is characteristic of the thermionic emission mechanism over the junction barrier. Conversely, the reverse bias current increases gradually without demonstrating a sharp or saturated breakdown regime (soft breakdown). This typical soft breakdown phenomenon is ascribed to the dominance of edge leakage currents across the contact peripheries and the field-assisted generation of excess charge carriers within the depletion layer at elevated reverse biases. Thermal annealing systematically controls the forward current onset, confirming the alteration of the junction barrier height in correlation with the C-V findings (Kumar and Chowdhury, 2017; Hameed et al., 2021).

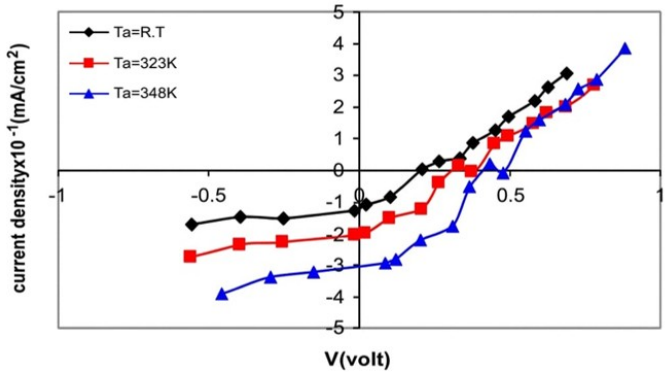

Figure 4. I-V Characteristics for TeSn/c-Si Heterojunction at Different Annealing Temperatures

3.4 Photovoltaic Performance under Illumination

The photoresponse and photovoltaic potential of the TeSn/c-Si heterojunction were investigated under light illumination. Figure 4 portrays the illuminated I-V profiles as a function of annealing temperatures. It is clearly observed that both the open-circuit voltage (V_{oc}) and the short-circuit current density (J_{sc}) experience a progressive rise as the annealing temperature of the TeSn film is raised.

The current density expands from 1.43×10^{-1} mA/cm^2 at Room Temperature to 2.09×10^{-1} mA/cm^2 at 323K, and reaches its peak value of 3.1×10^{-1} mA/cm^2 at 348 K. Physically, in the un annealed devices, structural defects and grain boundaries act as highly active recombination and capture centers for photo generated carriers, reducing the overall extraction efficiency. Thermal annealing at 323 K and 348 K significantly suppress these recombination centers by enlarging the crystalline grain size of the chalcogenide layer. As substantiated by recent photovoltaic reviewthe enlargement of grains lowers the grain-boundary scattering, allowing photo generated electron-hole pairs to be effectively separated by the enhanced built-in field (V_{bi}) and successfully collected at the electrodes, thereby boosting the net output current density which consequently enhances parameters governed by nanomaterial surface morphology modification as supported by related device structures reported in literature (Hussein et al., 2024; Ahmed et al., 2026; Ibrahim, 2009; Soundararajan and Mangalaraj, 2021; Jassim et al., 2024).

4. CONCLUSIONS

Thermal evaporation was used to prepare a heterojunction from the Te Sn/n-Si, which was heat-treated via post-deposition thermal annealing. The post-deposition thermal treatment at a temperature of 348 K resulted in a systematic improvement in the physical parameters of the device. The D.C. conductivity ($\sigma_{d.c}$) values confirmed the presence of a dual activation energy transfer mechanism, with a shift in activation energy values to 0.44 eV and 0.65 eV as a result of structural defects. Capacitance-voltage measurements (C-V) confirmed the sharp nature of the interface, revealing a significant expansion in the internal building potential (V_{bi}) from 1.24 eV to 1.7 eV at 348 K. Under illumination, the annealed junction at 348 K exhibited a superior photoresponse, maximizing the short-circuit current density (J_{sc}) to 3.1×10^{-1} mA/cm^2. These results proved that controlled thermal annealing is a viable model for improving the efficiency of chalcogenide-based solar harvesting devices.

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